SMA-001

Inventor: REDDY
Docket No.: SMA-001.1D
Title: INEXPENSIVE, RELIABLE, PLANAR RFID TAG STRUCTURE AND METHOD FOR MAKING SAME

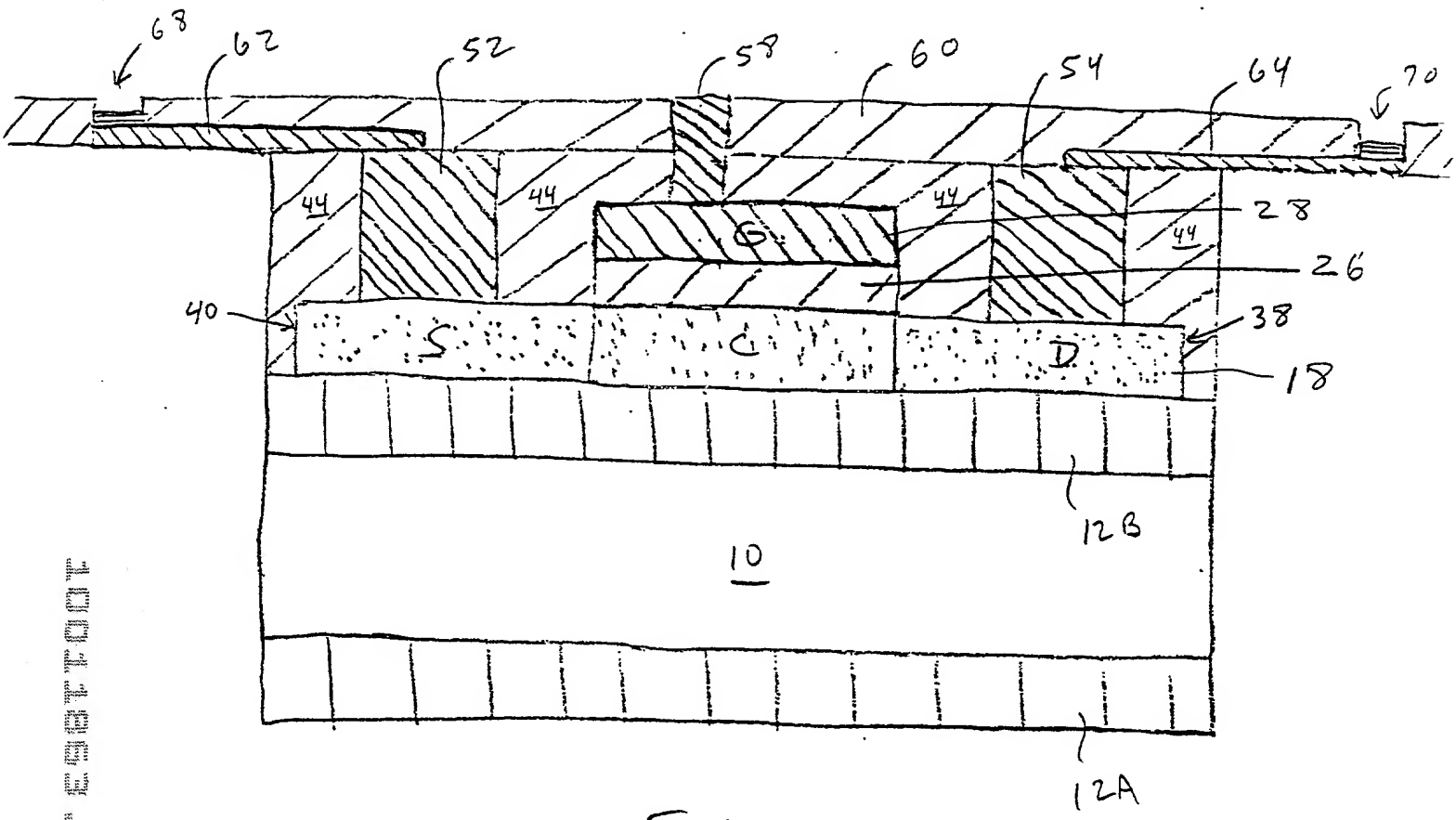

FIG. 1

(A)

Process Flow for Building Transistor Right Side up with Antenna on Top

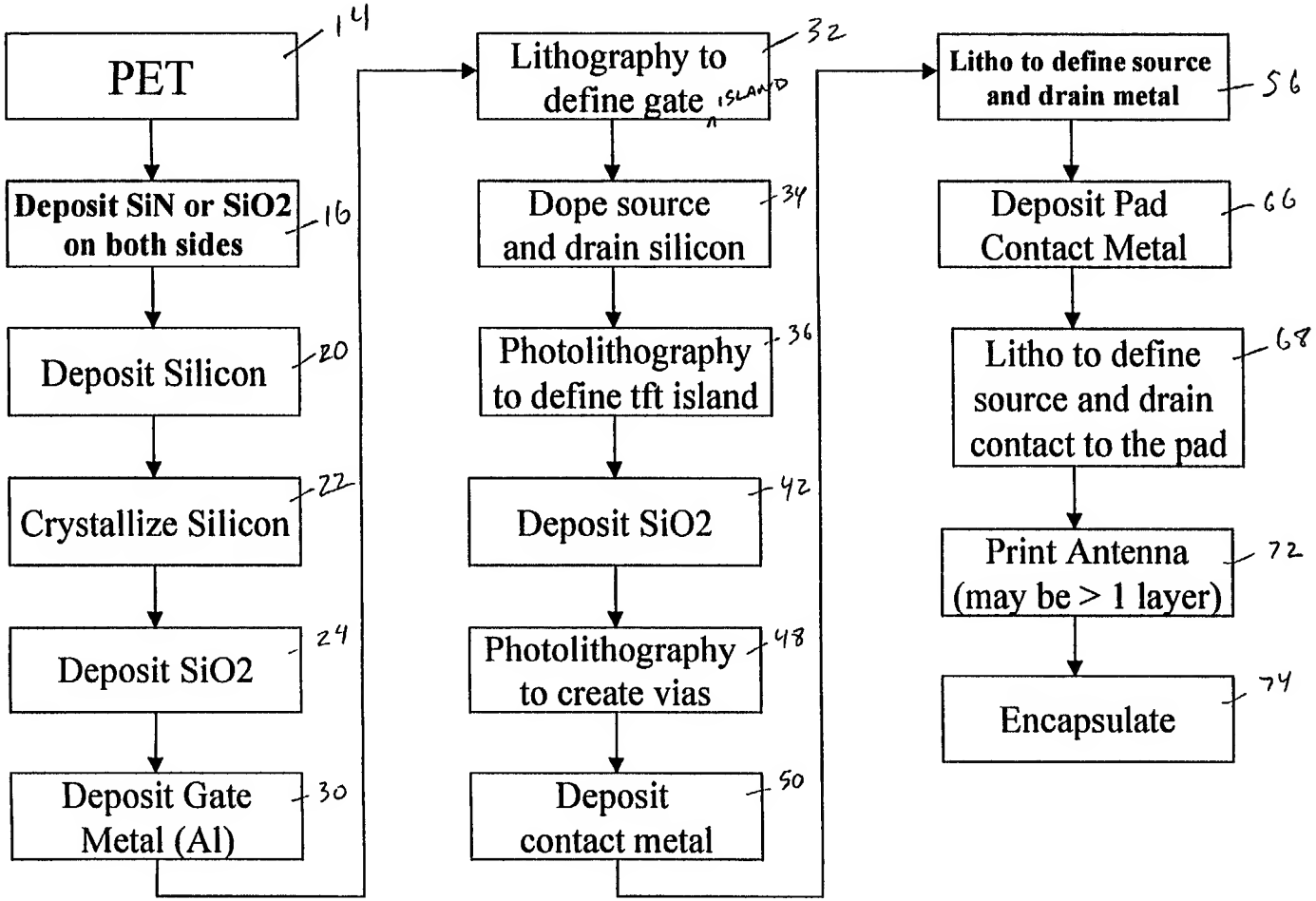

FIG. 2

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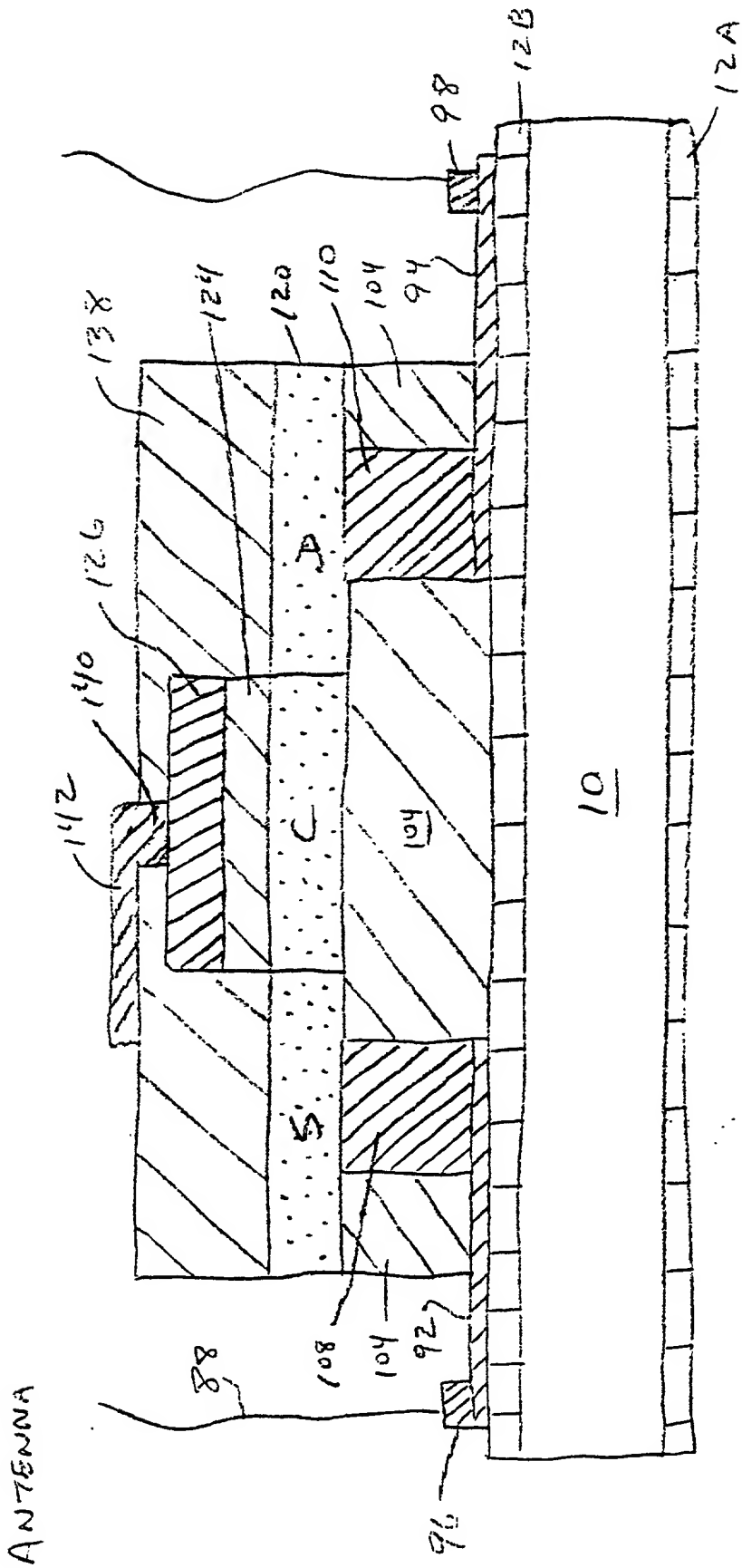

UPSIDE DOWN TRANSISTOR ON TOP OF PRINTED ANTENNA

FIG. 2

Process Flow for Building Transistor on Top of Antenna

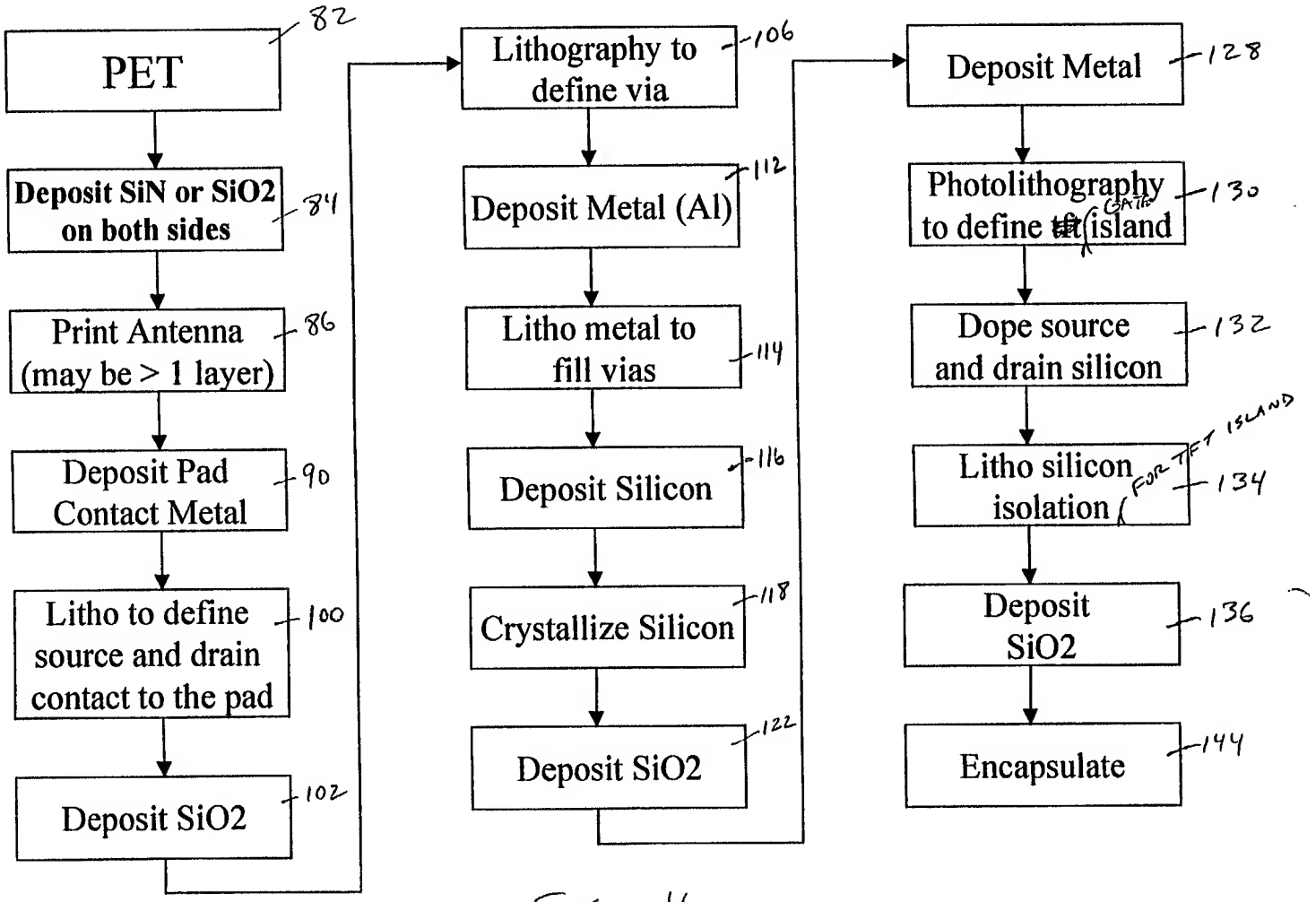

FIG. 4

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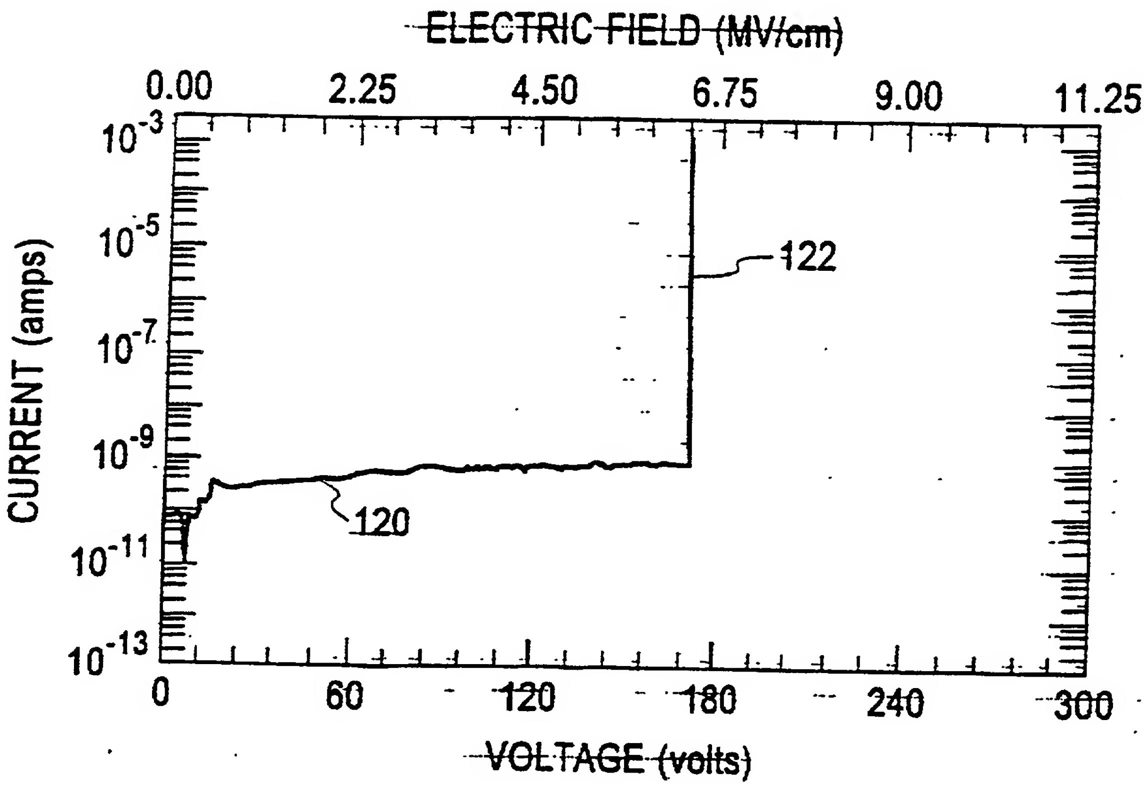


Fig. 5

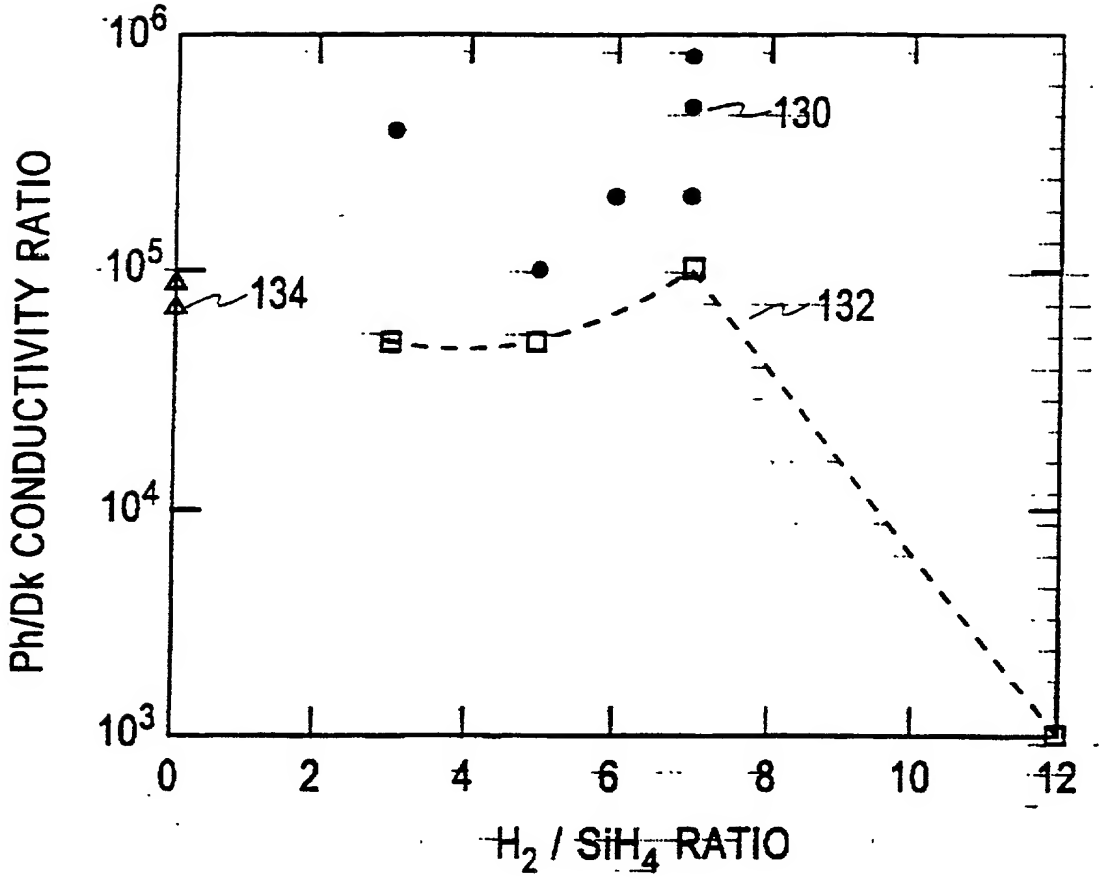

Ph/Dk CONDUCTIVITY RATIO
10^6
10^5
10^4
10^3
130
134
132
0
2
4
6
8
10
12
H_2 / SiH_4 RATIO

Fig. 6

Process Flow for Building EEPROM with Antenna on Top

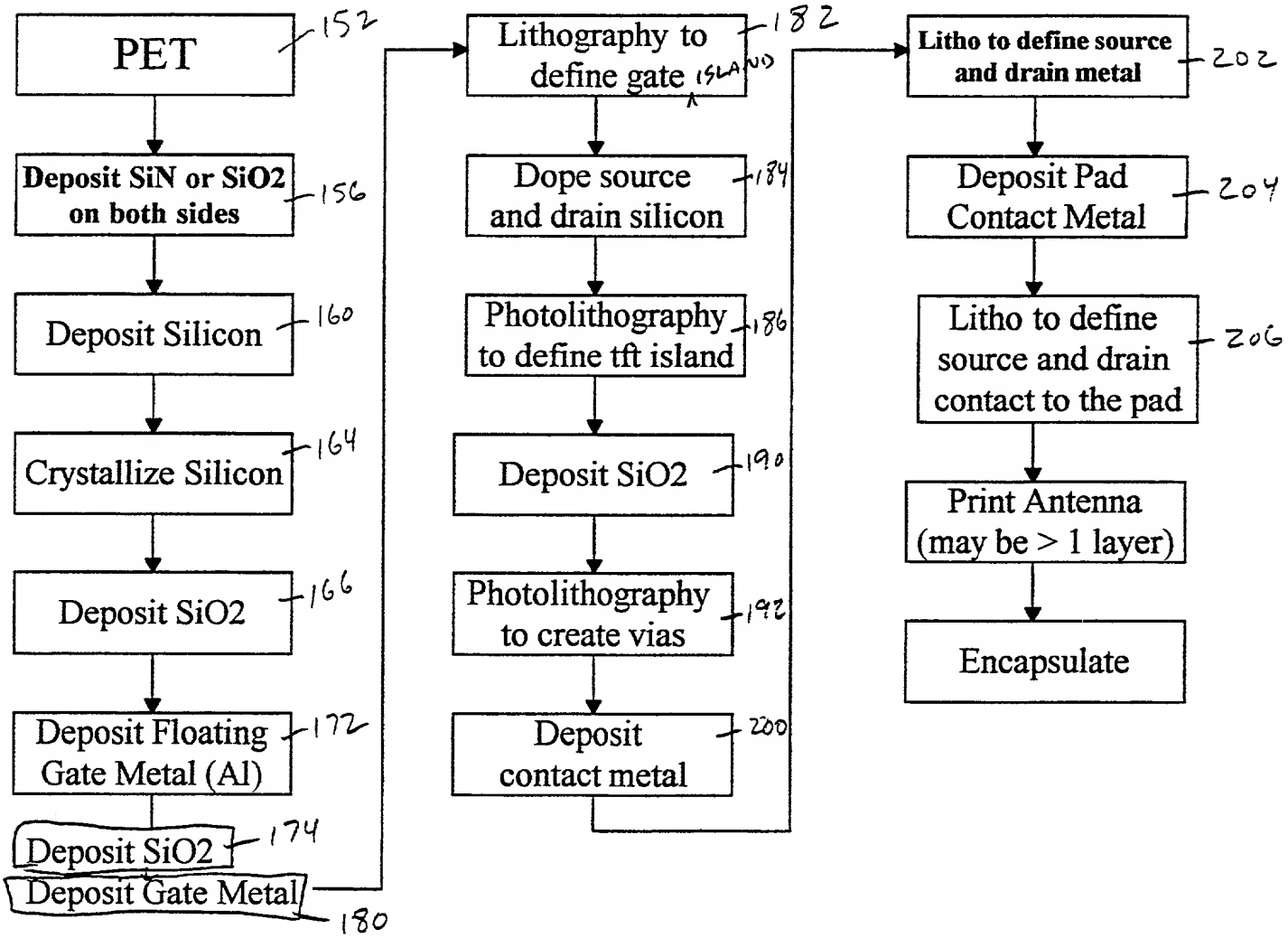
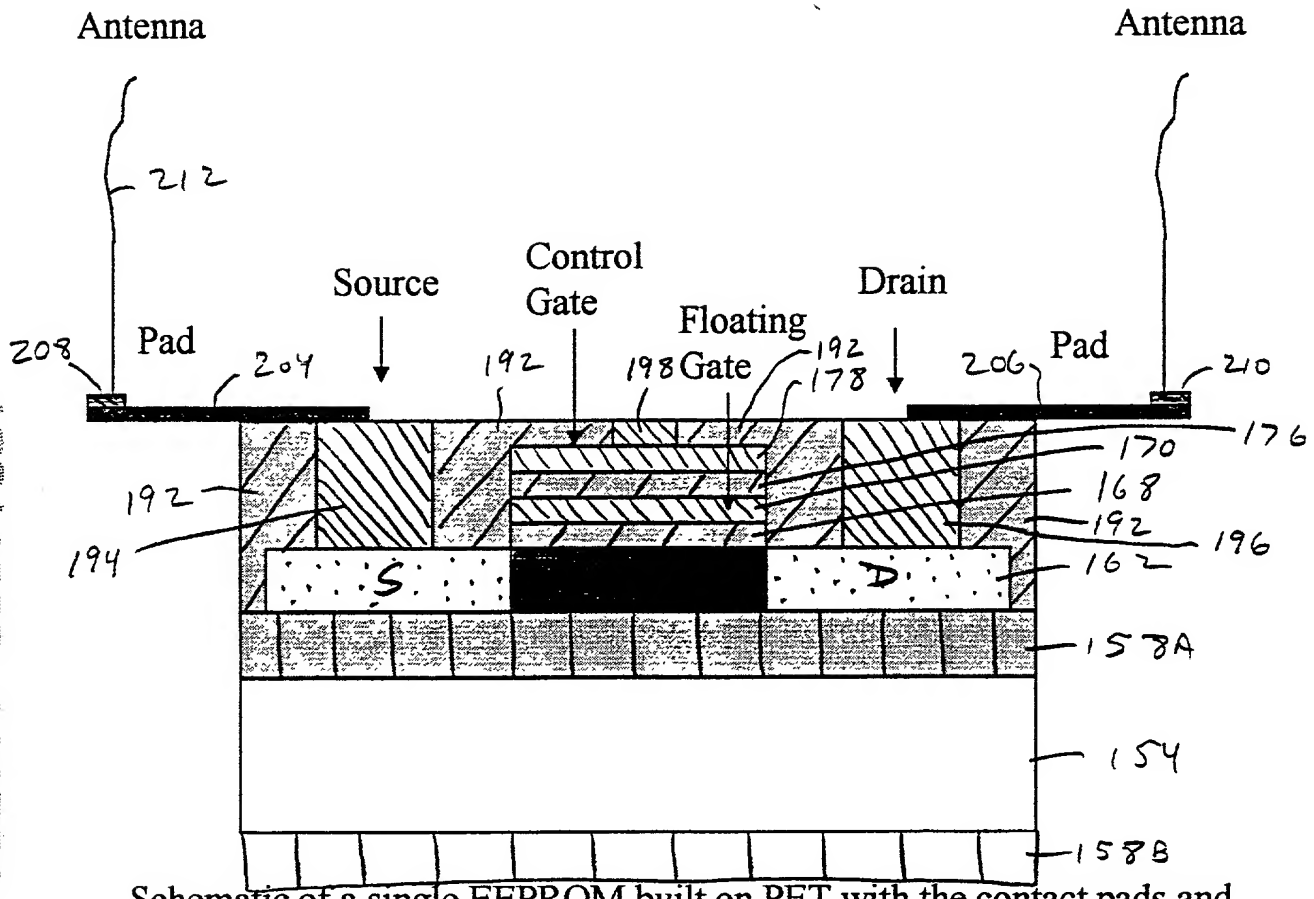


FIG. 7



Schematic of a single EEPROM built on PET with the contact pads and the antenna printed on top of the transistor; gate will be connected to the transistors (in actual devices multiple transistors and EEPROM will be connected to the contact pads)

FIG. 8

Process Flow for Building EEPROM on Top of Antenna

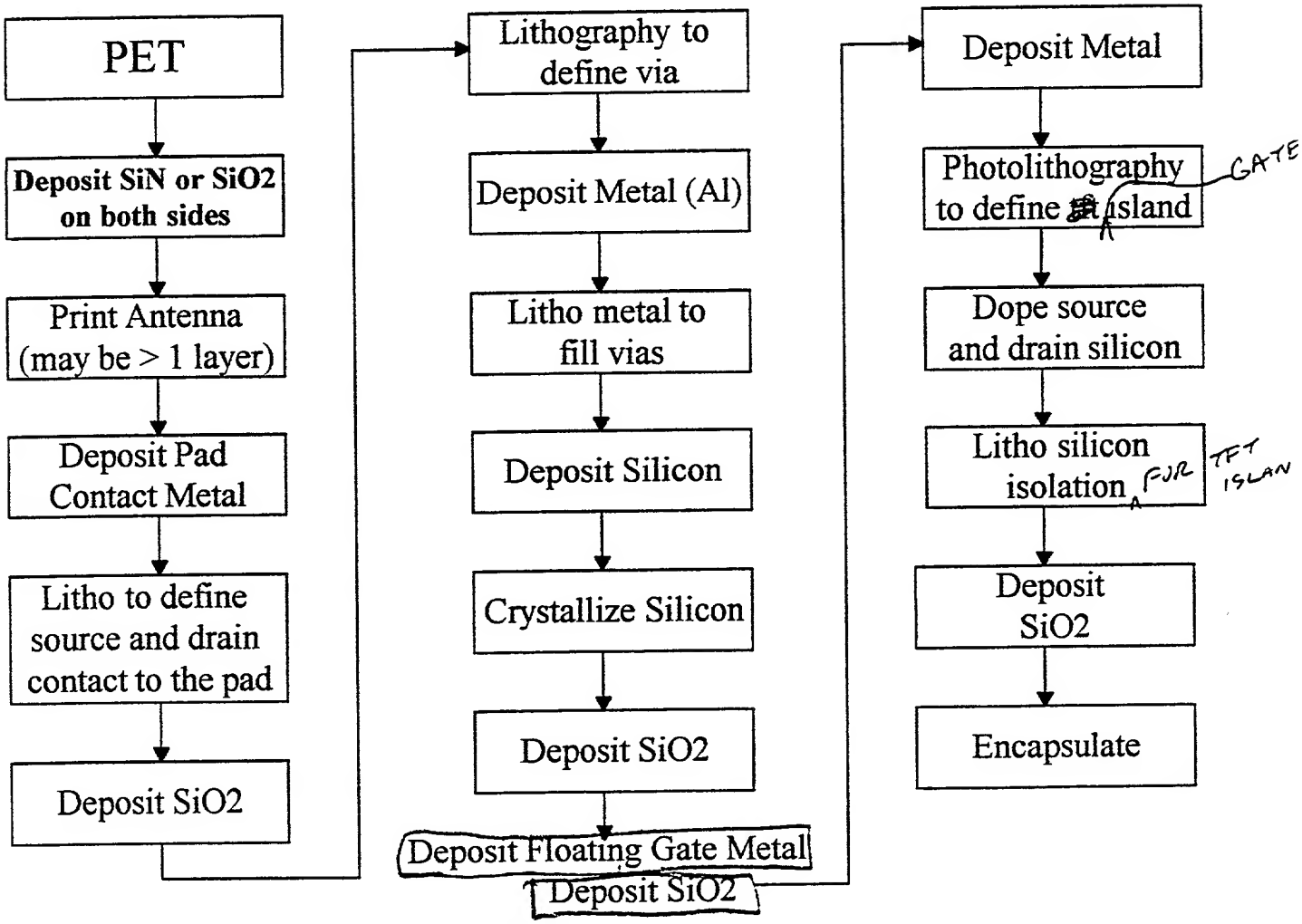
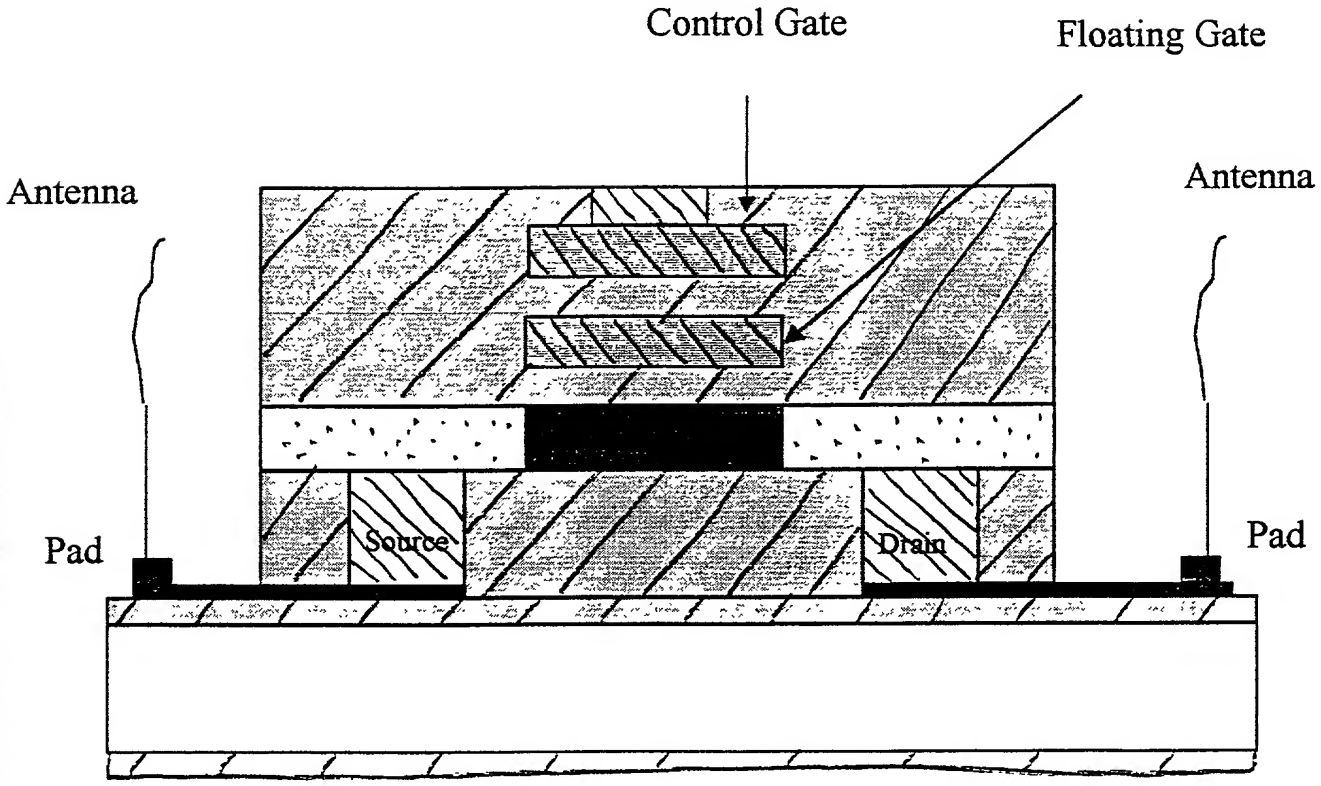


FIG. 9



Schematic of a single EEPROM built on top of the printed antenna
(in actual devices EEPROM and multiple transistors will be connected to the contact pads)

FIG. 10